Listing of Claims:

1. (Currently amended) A capacitor structure, comprising:

a substrate;

a conductive material formed above the substrate;

an insulating material formed on the conductive material, wherein the insulating material and the conductive material serve as a form for defining a plurality of capacitor trenches above the ~~metal layer~~ conductive material, the insulating material defining the trench sidewalls and the conductive material defining the trench bases;

a bottom electrode formed onto the capacitor trenches so as to form a layer within the capacitor trenches in contact with the conductive material, wherein the bottom electrode extends up the sides of the capacitor trenches to form bottom electrode sidewalls;

a capacitor dielectric at least partially positioned on the bottom electrode;

and

a top electrode at least partially positioned on the capacitor dielectric, substantially filling the capacitor trenches and forming an interconnect.

2. (Original) The capacitor structure of claim 1, wherein the capacitor dielectric is made from a material having a higher dielectric constant than the dielectric constant of the insulating material.

3. (Original) The capacitor structure of claim 1, wherein the capacitor dielectric has a high-k dielectric constant.

4. (Original) The capacitor structure of claim 3, wherein the capacitor dielectric has a dielectric

PAGE 9/21 * RCVD AT 3/22/2005 6:28:16 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:801 578 6999 * DURATION (mm-ss):05-14

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constant greater than or equal to about 6.0.

5. (Original) The capacitor structure of claim 1, wherein the capacitor dielectric comprises a stack comprising more than one material.

6. (Original) The capacitor structure of claim 1, wherein the capacitor structure is a discrete capacitor.

7. (Original) The capacitor structure of claim 1, wherein the capacitor structure is configured to be part of an integrated circuit.

8. (Canceled)

9. (Previously presented) The capacitor structure of claim 1, wherein the conductive material layer is comprised of a different material than the bottom electrode.

10. (Previously presented) The capacitor structure of claim 1, wherein the top electrode is at least partially disposed in the capacitor trenches such that the top electrode interdigitates with the bottom electrode.

11. (Original) The capacitor structure of claim 1, wherein the bottom electrode further comprises a bottom electrode top wall.

12. (Original) The capacitor structure of claim 11, wherein the bottom electrode further comprises a bottom electrode base.

13. (Withdrawn) A method for fabricating a capacitor structure, comprising:

etching a trench in a wafer, the wafer comprising a substrate, an insulating material, and a conductive material, wherein the conductive material is at least partially disposed within the insulating material, and wherein the trench is formed such that it contacts the conductive material;

forming a bottom electrode within the trench such that it is coupled to the conductive material, wherein the bottom electrode is formed such that it extends up the sides of the trench to form bottom electrode sidewalls;

depositing a capacitor dielectric within the trench on the bottom electrode; and

depositing a top electrode in the trench on the capacitor dielectric.

14. (Withdrawn) The method of claim 13, further comprising the step of depositing a protective topside layer on the wafer.

15. (Withdrawn) The method of claim 13, wherein the capacitor dielectric is made from a material having a higher dielectric constant than the dielectric constant of the insulating material.

16. (Withdrawn) The method of claim 13, wherein the capacitor dielectric has a high-k dielectric constant.

PAGE 11/21 * RCVD AT 3/22/2005 6:28:16 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:801 578 6999 * DURATION (mm-ss):05-14

17. (Withdrawn) The method of claim 16, wherein the capacitor dielectric has a dielectric constant greater than or equal to about 6.0.

18. (Withdrawn) The method of claim 13, wherein the capacitor dielectric comprises a stack comprising more than one material.

19. (Withdrawn) The method of claim 13, wherein the capacitor structure is a discrete capacitor.

20. (Withdrawn) The method of claim 13, wherein the capacitor structure is configured to be part of an integrated circuit.

21. (Withdrawn) The method of claim 13, wherein the capacitor structure is formed such that the conductive material is in contact with the bottom electrode.

22. (Withdrawn) The method of claim 21, wherein the conductive material layer is comprised of a different material than the bottom electrode.

23. (Withdrawn) The method of claim 13, wherein the top electrode is deposited so as to be at least partially disposed in the trench such that the top electrode interdigitates with the bottom electrode.

PAGE 12/21 * RCVD AT 3/22/2005 6:28:16 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:801 578 6999 * DURATION (mm-ss):05-14

24. (Withdrawn) The method of claim 13, wherein the bottom electrode is formed to further comprise a bottom electrode top wall.

25. (Withdrawn) The method of claim 24, wherein the bottom electrode is formed to further comprise a bottom electrode base.

26. (Original) A capacitor structure, comprising:

a substrate;

an insulating material formed on the substrate, wherein the insulating material serves as a form for defining a capacitor trench;

a bottom electrode, wherein the bottom electrode comprises a bottom electrode layer in the capacitor trench and a bottom electrode plug disposed within the capacitor trench, wherein the bottom electrode layer extends up the sides of the capacitor trench to form bottom electrode sidewalls;

a capacitor dielectric at least partially positioned on the bottom electrode and at least partially formed on the bottom electrode plug;

and

a top electrode at least partially positioned on the capacitor dielectric and at least partially formed around the bottom electrode plug.

27. (Original) The capacitor structure of claim 26, wherein the capacitor dielectric is made from a material having a higher dielectric constant than the dielectric constant of the insulating

material.

28. (Original) The capacitor structure of claim 26, wherein the capacitor dielectric has a high-k dielectric constant.

29. (Original) The capacitor structure of claim 26, wherein the capacitor dielectric has a dielectric constant greater than or equal to about 6.0.

30. (Original) The capacitor structure of claim 26, wherein the capacitor dielectric comprises a stack comprising more than one material.

31. (Previously presented) The capacitor structure of claim 26, wherein the capacitor structure is a discrete capacitor.

32. (Original) The capacitor structure of claim 26, wherein the capacitor structure is configured to be part of an integrated circuit.

33. (Original) The capacitor structure of claim 26, further comprising a conductive material layer, wherein the conductive material layer is in contact with the bottom electrode.

34. (Original) The capacitor structure of claim 33, wherein the conductive material layer is a different material than the bottom electrode.

35. (Original) The capacitor structure of claim 26, wherein the bottom electrode and the capacitor dielectric are formed in the shape of a box.

36. (Original) The capacitor structure of claim 26, wherein the top electrode is at least partially disposed in the capacitor trench such that the top electrode interdigitates with the bottom electrode.

37. (Original) The capacitor structure of claim 26, wherein the bottom electrode layer further comprises a bottom electrode top wall.

38. (Original) The capacitor structure of claim 37, wherein the bottom electrode layer further comprises a bottom electrode base.

39. (Withdrawn) A method for fabricating a capacitor structure, comprising:

etching a trench in a wafer, the wafer comprising a substrate, an insulating material, and a conductive material, wherein the conductive material is at least partially disposed within the insulating material, and wherein the trench is formed such that it contacts the conductive material;

depositing a bottom electrode layer in the trench such that the bottom electrode layer is coupled to the conductive material and such that the bottom electrode layer extends up the sides of the trench to form bottom electrode sidewalls;

depositing sacrificial material in the trench, wherein the sacrificial material is deposited such that the trench is not fully occupied by the sacrificial material;

PAGE 15/21 * RCVD AT 3/22/2005 6:28:16 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:801 578 6999 * DURATION (mm-ss):05-14

depositing a bottom electrode plug in the trench, wherein the bottom electrode plug is deposited in the trench such that the bottom electrode plug contacts the conductive material;

removing substantially all of the sacrificial material from the trench;

depositing a capacitor dielectric in the trench on the bottom electrode layer and the bottom electrode plug; and

depositing a top electrode in the trench on the capacitor dielectric.

40. (Withdrawn) The method of claim 39, wherein the trench is formed in the shape of a box.

41. (Withdrawn) The method of claim 39, further comprising the step of etching the sacrificial material from at least a portion of the bottom of the trench.

42. (Withdrawn) The method of claim 39, further comprising the step of depositing a protective topside layer on the wafer.

43. (Withdrawn) The method of claim 39, wherein the capacitor dielectric is made from a material having a higher dielectric constant than the dielectric constant of the insulating material.

44. (Withdrawn) The method of claim 39, wherein the capacitor dielectric has a high-k dielectric constant.

PAGE 16/21 * RCVD AT 3/22/2005 6:28:16 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:801 578 6999 * DURATION (mm-ss):05-14

45. (Withdrawn) The method of claim 44, wherein the capacitor dielectric has a dielectric constant greater than or equal to about 6.0.

46. (Withdrawn) The method of claim 39, wherein the capacitor dielectric comprises a stack comprising more than one material.

47. (Withdrawn) The method of claim 39, wherein the capacitor structure is a discrete capacitor.

48. (Withdrawn) The method of claim 39, wherein the capacitor structure is configured to be part of an integrated circuit.

49. (Withdrawn) The method of claim 39, wherein the bottom electrode layer and the bottom electrode plug comprise the same material, and wherein the material of the bottom electrode layer and the bottom electrode plug is different than the material of the conductive material.

50. (Withdrawn) The method of claim 39, wherein the top electrode is deposited so as to be at least partially disposed in the trench such that the top electrode interdigitates with the bottom electrode.

51. (Withdrawn) The method of claim 39, wherein the bottom electrode layer further comprises a bottom electrode top wall.

PAGE 17/21 * RCVD AT 3/22/2005 6:28:16 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:801 578 6999 * DURATION (mm-ss):05-14

52. (Withdrawn) The capacitor structure of claim 51, wherein the bottom electrode further comprises a bottom electrode base.

53. (Withdrawn) A method for fabricating a capacitor structure, comprising:

etching a trench in a wafer, the wafer comprising a substrate, an insulating material, and a conductive material, wherein the conductive material is at least partially disposed within the insulating material, and wherein the trench is formed such that it contacts the conductive material;

depositing a second conductive material in the trench;

etching the second conductive material such that a bottom electrode plug is left in the trench;

depositing a bottom electrode layer in at least a portion of the trench surrounding the bottom electrode plug;

depositing a capacitor dielectric in the trench on the bottom electrode layer and the bottom electrode plug; and

depositing a top electrode in the trench on the capacitor dielectric.

54. (Withdrawn) The method of claim 53, wherein the bottom electrode layer and bottom electrode plug comprise the same material.

PAGE 18/21 * RCVD AT 3/22/2005 6:28:16 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:801 578 6999 * DURATION (mm-ss):05-14

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